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01/09/2002

PATENT NUMBER and  
ISSUE DATE

U.S. UTILITY Patent Application

APPL NUM 10043763	FILING DATE 01/09/2002	CLASS 327	SUBCLASS 534	GAU 3816 2956	EXAMINER Cunningham
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APPLICANTS: Ajit Janardhanan;

\*\*CONTINUING DATA VERIFIED:

THIS APPLN CLAIMS BENEFIT OF 60/260,580 01/09/2001  
AND CLAIMS BENEFIT OF 60/260,582 01/09/2001

TDC

\*\* FOREIGN APPLICATIONS VERIFIED:

NONE  
TDC

PG-PUB DO NOT PUBLISH <input type="checkbox"/>	RESCIND <input type="checkbox"/>
Foreign priority claimed <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	ATTORNEY DOCKET NO
35 USC 119 conditions met <input type="checkbox"/> yes <input checked="" type="checkbox"/> no	41980/RJP/B600
Verified and Acknowledged Examiners's initials	
TITLE : Sub-micron high input voltage tolerant input output (I/O) circuit which accommodates large power supply variations	

U.S. DEPT. OF COMM/PAT. & TM-PTO-436L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED		CLAIMS ALLOWED	
		Total Claims	Print Claim for O.G.
Assistant Examiner			
ISSUE FEE		DRAWING	
Amount Due	Date Paid	Sheets Drawn	Figs Drawn
		Print Fig.	
<input type="checkbox"/> TERMINAL DISCLAIMER		Primary Examiner PREPARED FOR ISSUE Application Examiner	
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